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Stylesheet Version v1.1.1

Description

INTEGRATED CIRCUIT DESIGN SYSTEM

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an integrated circuit, and more particularly, to an integrated circuit design system for designing an application-specific integrated circuit (ASIC).

[0003] 2. Description of the Prior Art

[0004] In accordance with the rapid development of electronic technologies, many complicated circuits can be integrated into an integrated circuit (IC) to save space in an electronic apparatus having complicated design. Integrated circuit design systems are used to design ICs.

[0005] Please refer to Fig.1, which is a flow chart of a method 100 demonstrating how an integrated circuit design system designs an application-specific integrated circuit (ASIC) according to the prior art. The method 100 comprises the following steps:

[0006] Step 102:Start;

[0007] Step 104:Logic design & synthesis;

[0008] (Logic designers input hardware description language (HDL) to the integrated circuit design system to form a first netlist, and transfer the first netlist and timing constraints corresponding to the ASIC to physical designers.)

[0009] Step 106:Placement & routing;(The physical designers execute a variety of processes, such as a placement & routing process, a clock tree synthesis process, a timing optimization process, and a cell and wire delay extraction process, on an IC chip according to the first netlist and the timing constraints transferred from the logic designers to update the first netlist to a second netlist; and transfer the second netlist and corresponding cell and wire delay information in standard delay format (SDF) back to the logic designers.)

[0010] Step 108:Timing analysis & functional verification, if successful, go to step 190, else go to step 110;(The logic designers check the SDF and the second netlist to determine if the second netlist violates the timing constraints or any function that the ASIC should have.)

[0011] Step 110:Netlist update; and

[0012] (The method 100 coming thus far indicates that the second netlist transferred by the physical designers still has some errors existing in either the timing constraints or the function, so the logic designers therefore have to correct the errors by updating the second netlist and transfer the updated second netlist to the physical designers. The physical designers must execute a corresponding engineering change order (ECO) again.)

[0013] Step 190:End.

[0014] According to the scenario described above, a netlist such as an N_{th} netlist shown in Fig.1 has to be transferred back and forth between the logic designers and the physical designers until all the errors of the N_{th} netlist have been corrected.

SUMMARY OF INVENTION

[0015] It is therefore a primary objective of the claimed invention to provide an integrated circuit design system to solve the drawbacks of the prior art.

[0016] According to the claimed invention, the integrated circuit design system includes a second interface for displaying a plurality of description instructions corresponding to an application-specific integrated circuit (ASIC) according to

a variety of display instructions, a first interface for inputting the display instructions and for updating the description instructions displayed on the second interface according to the display instructions, and a logic unit for updating any description instruction but an updated description updated by the first interface corresponding to the ASIC according to the updated description instruction.

[0017] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0018] Fig.1 is a flow chart of a method demonstrating how an integrated circuit design system designs an ASIC according to the prior art.

[0019] Fig.2 is a schematic diagram of an IC chip of the preferred embodiment according to the present invention.

[0020] Fig.3 is a schematic diagram of an ASIC of the IC chip shown in Fig.2 according to the present invention.

[0021] Fig.4 is a schematic diagram of an integrated circuit design system of the preferred embodiment according to the present invention.

[0022] Fig.5 is an enlarged view of a plurality of elementary cells encircled within a dotted line shown in Fig.3 on a physical circuit window shown in Fig.4.

DETAILED DESCRIPTION

[0023] Please refer to Fig.2, which is a schematic diagram of an integrated circuit chip 10 of the preferred embodiment according to the present invention. The integrated circuit chip 10 comprises a semiconductor substrate 12, a plurality of elementary cells 14 installed on the semiconductor substrate 12, and a plurality of interconnects 18 for connecting the elementary cells 14.

[0024] In general, in a process of designing an ASIC 50, a plurality of the elementary cells 14 installed neighboring to one another can be arranged to form a macro cell having a specific function. Please refer to Fig.3, which is a schematic diagram of the ASIC 50 of the integrated circuit chip 10 shown in Fig.2. The ASIC 50 comprises a plurality of elementary cells 14, a plurality of interconnects 18, a clock generator 52, two DRAMs 54, a read-only memory (ROM) 56, a CPU 58, an input/output unit 60, and a plurality of macro cells, each of which is composed of a plurality of elementary cells 14.

[0025] Please refer to Fig.4, which is a schematic diagram of an

integrated circuit design system 20 of the preferred embodiment according to the present invention. The system 20 comprises a first interface 22, a second interface 26, and a logic unit 24 electrically connected between the first and second interfaces 22 and 26.

[0026] The first interface 22 is installed for a user to input display instructions and to update information related to ASIC 50 of a variety of reports, such as a netlist, a noise analysis report, a power analysis report, and a timing slack report, etc.

[0027] The logic unit 24 is installed to execute a variety of processes, such as a placement & routing process, a clock tree synthesis process, a timing optimization process, and a cell and wire delay extraction process, etc., on the integrated circuit chip 10 according to the information updated through the first interface 22 by the user, and to further generate an updated netlist, an updated noise analysis report, an updated power analysis, an updated timing slack report, and an updated cell and wire delay extraction report.

[0028] In operation, for example, if a netlist of the ASIC 50 has been updated by a logic designer with the use of the first interface 22, then the logic unit 24 will execute the place-

ment & routing process, the clock tree synthesis process, the timing optimization process, and the cell and wire delay extraction in accordance with the updated netlist, and generate a variety of information relating to the ASIC 50, such as the updated noise analysis report, the updated power analysis, the updated timing slack report, and the updated cell and wire delay extraction report, according to the updated netlist. In another example, if what the logic designer has updated through the use of the first interface 22 is circuit component information of the timing slack report of the ASIC 50, the logic unit 24 will generate another updated noise analysis report, another updated power analysis, another updated netlist, and another updated cell and wire delay extraction according to the updated circuit component information of the timing slack report, and all of the updated noise analysis report, the updated power analysis, the updated netlist, and the updated cell and wire delay extraction relating to the updated circuit component information of the timing slack report. Equivalently, the integrated circuit design system 20 transforms the ASIC 50 into a core database consisting of the above-mentioned information, any updated information of the core database providing an influence on the

remaining information.

[0029] In the core database, the timing slack report comprises a plurality of timing slack information, each of which comprises a plurality of timing slacks S_ss, each of the timing slacks S_ss equal to a required time R_s, within which a signal S has to be stabilized, minus an arrival time A_s, the time for the signal S to be stabilized. If the timing slack S_s is positive, the signal S has been stabilized before arriving at other circuits, such as a latch capable of fetching the signal S during a rising edge of a driving clock, when the signal S has been stabilized. On the contrary, if the timing slack S_s is negative, the signal S is not stabilized during the rising edge of the driving clock and the latch has therefore a large chance of fetching a wrong signal S. The benefit of the logic unit 24 calculating the timing slack information is that the logic designer can update the netlist with the use of the first interface 22 in accordance with the timing slack information, and instantly acquire new timing slack information, which are calculated by the logic unit 24 and corresponding to the updated netlist, so as to promote the efficiency in designing the ASIC 50 and to reduce any potential errors that the ASIC 50 may have.

[0030] The second interface 26 is installed to display the varieties

of information of the core database in accordance with the display instructions. These varieties of information comprise, for example, a netlist, an updated netlist, and a plurality of the netlist- or the updated netlist-related reports, such as a placement & routing report, a clock tree synthesis report, a timing optimization report, and a cell and wire delay extraction report, etc.

[0031] In the preferred embodiment, the second interface 26 only has to display the negative timing slacks S_ss of the timing slack information calculated by the logic unit 24, instead of displaying all of the timing slack S_ss, which consist of not only the negative timing slacks S_ss, but also the positive timing slacks S_ss, which correspond to signals which are not stable and have a large chance of induced errors, so as to reduce the complexity of the integrated circuit design system 20.

[0032] In the preferred embodiment, the first interface 22 can be a keyboard 22 or a mouse 22, and the second interface 26 can be a display panel 26, on which the above-mentioned information, such as the netlist and the timing slack report, can be displayed in the form of a window. Shown in Fig.4 are a noise analysis report window 32 for illustrating the noise analysis report corresponding to the ASIC 50, a

netlist window 34 for illustrating the netlist corresponding to the ASIC 50, a physical circuit window 36 for illustrating the placement & routing of the integrated circuit chip 10 corresponding to the netlist, and a timing slack report window 38 for illustrating the timing slack report corresponding to the netlist generated by the logic unit 24, the timing slack report shown on the timing slack window 38 comprising the negative timing slacks S_ss only.

[0033] According to the prior art described previously, after updating a netlist according to timing slack information transferred from the physical designers, the logic designers are not able to refer to any physical circuit information corresponding to the timing slack information and cannot know immediately whether the timing slack problem corresponding to a physical circuit corresponding to the updated netlist is solved or not, so the logic designers and the physical designers still have to alternatively update the netlist in accordance with the timing slack information, update the physical circuit in accordance with the updated netlist, and calculate the timing slack information corresponding to the updated physical circuit.

[0034] However, according to the preferred embodiment of the present invention, the first interface 22 is capable of up-

dating any information of the core database, which is in equivalent corresponding to the ASIC 50, the logic unit 24 is capable of updating the remaining information of the core database according to the updated information, and the display panel 26 is capable of displaying the noise analysis report on the noise analysis report window 32, the netlist on the netlist window 34, the layout of the ASIC 50 on the physical circuit window 36, and the timing slack report corresponding to the netlist of the ASIC 50 on the timing slack report window 38 in accordance with the display instructions input to the keyboard 22 or the mouse 22. The logic designers therefore are able to update the circuit component information shown on any one of the windows 32, 34, 36 and 38, without the need to ask for the help offered by the physical designers.

[0035] Please refer to Table 1, which contains a timing slack information TS shown in the timing slack window 38.

[0036] Table 1

[0037] _

[0038]

		Incr	Path
clock	SYSCK266	0	0
	CGEN_A_PST/PST_ff_0/CK	0	0
	CGEN_A_PST/PST_ff_0/Q	0.54	0.54
	CGEN_A_PST/I_62/Y(NAND2x1)	0.18	0.72
	CGEN_A_PST/I_23/Y(BUFx4)	0.07	0.79
	CGEN_A_PST/I_42/Y(BUFx8)	0.06	0.85
	CGEN_A_PST/I_12/Y(AND2x1)	0.15	1.0
	CGEN_A_PST/PST_ff_1/D(SDFFRX1)	0	
	data arrival time		1.0
clock	SYSCLK266	5	5
	CGEN_A_PST/PST_ff_1/CK	0	5
	library setup time	-0.12	4.88
	data required time		4.88
	slack(TS)		3.88

[0039] _

[0040] The timing slack TS is equal to a required time Rs minus an arrival time As, which is the sum of delay time of a plurality of components disposed along a data path. In Table 1, the arrival time As is equal to 0.54+0.18+0.07+0.06+0.15=1.0, and the timing slack TS is equal to 4.88-1.0=3.8. After a logic designer updates the netlist corresponding to the ASIC 50, the logic

unit 24 will update a timing slack report, which includes the delay time of each of the components, the required time Rs, the arrival time As and the timing slack TS, corresponding to the updated netlist in accordance with the updated netlist. The logic designer can therefore input a set of specific display instructions to enable the second interface 26 to display the timing slack report window 38, to read on the timing slack report window 38 an updated timing slack report corresponding to the updated netlist. The logic designer can also update circuit component information shown in the timing slack report window 38 through the use of the first interface 22 to reduce the slack time TS by equivalently inserting an approximate component between two pieces of data path information, CGEN_A_PST/I_62/Y(NAND2x1) and CGEN_A_PST/I_23/Y(BUFx4) respectively corresponding to two delay times (0.18) and (0.07). Accordingly, the logic unit 24 will update the remaining information of the core database according to the updated circuit component information, and the logic designer can input certain display instructions to enable the second interface 26 to display the netlist window 34 or the physical circuit window 36, and can read the updated netlist shown on the netlist

window 34 or execute the placement & routing process on the physical circuit shown on the physical circuit window 36.

[0041] In general, the timing slack report that the logic unit 24 generates in accordance with the execution on the placement & routing process, the clock tree synthesis report and the timing optimization report comprises much information. In order to accelerate the update to the timing slack report, the logic unit 24 of the system 20 further has a capacity to classify the timing slack report according to the contents of the timing slack report and divide a large timing slack report into a plurality of small timing slack reports. Therefore, more than one logic designer can cooperate to update the plurality of small timing slack reports at the same time. The logic unit 24 can classify the timing slack report by referring to the circuit components of the timing slack report or to the clock that the timing slack report corresponds.

[0042] According to the preferred embodiment, the logic unit 24 not only has the capability to calculate the noise analysis report, power analysis report and timing slack report corresponding to an updated netlist, the logic unit 24 is also capable of referring the updated circuit component infor-

mation shown on any window and of updating the information shown on the remaining windows. As described previously, the logic designers can update the circuit component information of the timing slack information shown on the timing slack window 36, and at the same time the logic unit 24 will update the netlist and the physical circuit according to the updating process on the circuit component information of the timing slack information, the updated netlist and physical circuit will be shown on the netlist window 34 and the physical circuit window 36 respectively. Moreover, since the circuit is updated, the logic unit 24 will further update the information shown on the remaining windows, such as the timing slack report, the power analysis report and the noise analysis report, etc. In conclusion, the logic designers of the system 20 can select any window and execute the updating process on the circuit shown on the selected window, and the logic unit 24 of the system 20 will accordingly update the information shown on the remaining windows according to the updating process.

[0043] In general, since the IC chip 10 can consist of up to millions or tens of million elementary cells 14, the system 20 does not display all the elementary cells 14 on the display

panel 26 in great detail. Instead, the system 20 displays on the display panel 26 only those elementary cells 14 and the interconnects 18 connecting the displayed elementary cells 14 which are corresponding to a netlist or a timing slack S_s according to the display instructions input to the first interface 22, for example clicking the mouse 22 to select the netlist shown on the netlist window 34.

[0044] For instance, when a logic designer selects a circuit description instruction in a netlist set consisting of a plurality of netlist instructions shown on the netlist window 34, a elementary cell 14 in a physical circuit consisting of a plurality of elementary cells shown on the physical circuit window 36, or circuit component information corresponding to a timing slack S_s in a timing slack report consisting of a plurality of timing slack S_ss shown on the timing slack window 36 with the use of the mouse 22 by generating a corresponding display instruction, the system 20 will control the display panel 26 to highlight the circuit description instruction, the elementary cell 14, or the elementary cells 14 and the corresponding interconnects 18 of the IC chip 10 corresponding to the circuit component information corresponding to the timing slack S_s of the timing slack information according to the display instruction. In

addition, the system 20 is capable of controlling the display panel 26 to display a plurality of spare cells 28 neighboring the highlighted elementary cells 14, the spare cells 28 being the elementary cells 14 not yet utilized by the system 20. Therefore, the logic designers can take a reference of the elementary cells, the interconnects 18 and the spare cells 20 and update the netlist to amend any design errors hid in the timing slack information corresponding to the ASIC 50.

[0045] Please refer to Fig.5, which is an enlarged view of a plurality of elementary cells 14 encircled within a dotted line shown in Fig.3 on the physical circuit window 36. As described previously, as the logic designers click the mouse 22 to generate a display instruction by selecting the circuit component information corresponding to a timing slack generate a display instruction to S_s of the timing slack information, the system 20 will display on the display panel 18 the elementary cells 14 and the interconnects 18 connected between the elementary cells 14, which are corresponding to the circuit component information. As shown in Fig.5, the circuit component information corresponding to the negative timing slack S_s that the logic designers have selected are corresponding to the

elementary cell A_{31} and the elementary cell A_{46}, which is electrically connected to the elementary cell A_{31} through the interconnect L_1. The signal S to be transferred from the elementary cell A_{46} to the input/output unit 60 is not stabilized yet. According to the preferred embodiment, in addition to the elementary cell A_{31}, the interconnect L_1, which is shown in Fig.5 in the form of a dotted line, and the elementary cell $A_{46,}$ the display panel 26 is capable of further displaying the spare cells 28 such as the spare cell A_{24}, which is disposed neighboring the elementary cell A_{31} as well as the elementary cell A_{46}, according to the display instructions, so that the logic designers are therefore able to execute on the physical circuit window 36 the updating process to reconnect the elementary cell A_{31} to the elementary cell A_{46} through a new path consisting of an interconnect L_2, an elementary cell A_{23}, an interconnect L_3, an elementary cell A_{24}, and an interconnect L_4, to transform the negative timing slack S_s into a positive timing slack S_s and to guarantee that the ASIC 50 can operate normally. Of course, after the logic designers have updated the physical circuit, the core database will be updated accordingly, and the netlist, the timing slack report, the noise analysis report and the power analysis report

will be updated too.

[0046] In order to increase the readability of the system 20 further, the display panel 26 is capable of selectively displaying a variety of icons, each of the icons corresponding to a elementary cell 14 of the ASIC 50 and having a predetermined pattern corresponding to a predetermined function that the elementary cell 14 plays in the ASIC 50. For example, as shown in Fig.5 three elementary cells A_{52}, A_{64}, and A_{52} having latching, inverting, and buffering functions respectively are shown to have a latch, an inverter, and a buffer pattern on the physical circuit window 36 of the display panel 26.

[0047] In contrast to the prior art, the present invention can provide an integrated circuit design system capable of displaying all the information of the core database corresponding to the ASIC 50. Therefore, a logic designer can refer to the timing slack report or the function verification report and not only update the netlist, the logic designer can also acquire a variety of information relating to the ASIC 50, such as the placement & routing information and the updated netlist, so as to reduce the time to update the netlist and to increase the efficiency of designing the ASIC 50.

[0048] Following the detailed description of the present invention above, those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.